Final Report of OTKA No. 109232 Research project

In the following chapters, the results of the research work in frame of OTKA No. 109232 national project are summarized. The different activities which were fulfilled in different work packages are presented in separate chapters.

1 WP1 – Manufacturing technologies

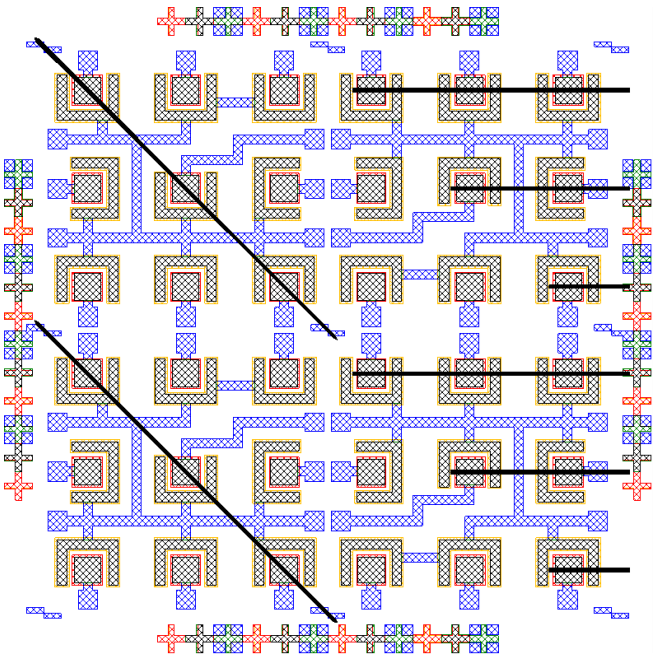
Within the frame of WP1 the processing of CMOS compatible integrated microscale heatsink structures was done. The technology setup was elaborated and several experimental setups for wet etching were carried out. It was followed by the realization of different channel patterns and the development of process steps for integrating microscale heat sink structure into semiconductor devices. Finally, some prototypes were developed. Since the samples was provided by WP1 had close interaction with other WPs. The results of the WP2 influenced the layout of the channels in the microscale heatsink structures. Forasmuch, WP3 mainly focused on the measurement of the developed heatsink structures it leaned on the results of WP1. It is somewhat evident since the built-up of the support structure applied in measurements determined the geometric dimensions and set-up of the investigated structures.

The key contribution of WP1 to the project was the elaboration of the CMOS compatible integrated manufacturing technology since the microscale heatsink are aimed to be used on the back side of high yield, high performance devices so the applicability must be demonstrated. [1]-[3]

By applying CMOS compatible wet chemical etching process realizing integrated microscale channel structures several sample devices were created. The detailed technology setup was elaborated and devices with different channel patterns were fabricated. In the first phase of the research, microcooler devices with radial channel patterns were created and covered using anodic bonding. The layout of the devices was similar to a formerly realized microscale cooler structure which was manufactured by using LIGA process. This way the results were comparable.

Based on our simulations, analytical modelling and calculation new channel architecture and layout were developed and the necessary chrome mask sets were designed and manufactured. Some of the new channel patterns were designed not to achieve the highest heat removal capability but for the fine tuning of the modelling and characterization technique. The new integrated microscale heatsink structures with the new channel patterns were realized on (100) orientation silicon wafers which resulted in steeper channel walls and higher Nusselt number and heat exchange ratio. The realized structures can be applicable for liquid and gas fluid as well, so the applicability and integrability of this structure into a System-on-Package device will be ensured.

At this point, it must be emphasized that since the System-on-Package integration is not a straightforward task, many fabrication steps have to be fully developed before a successful chip-level cooling system is ready to be used. In the frame of the project OTKA No. 109232 a refined manufacturing technology had to be developed and presented which gives the possibility to create the microscale heatsink structures integrated together with the electronic devices.



–n+ diffusion mask

–p diffusion mask

–Contact window mask

–Metallization mask

–TMAH etching mask on the back side for microchannel formation

Figure 1 – Compact drawing showing all lithographic masks superimposed - the heat dissipating devices over the diagonal channels (top-left and bottom-left chips), 3 simple channels with different lengths (top-right and bottom-right chips)

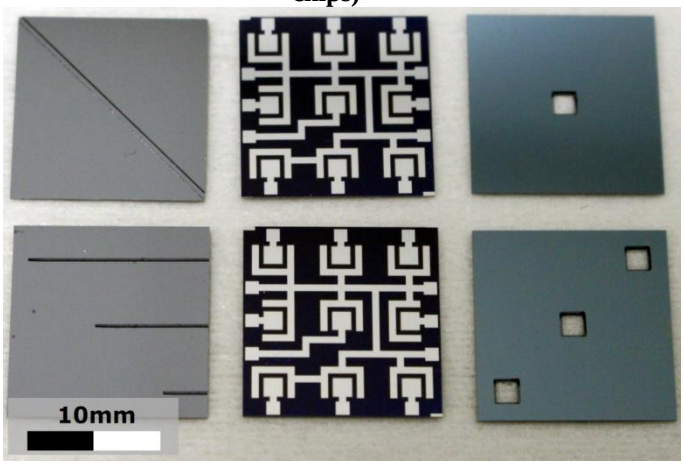


Figure 2 – Finished devices from left to right: the front sides of the integrated devices containing the microscale channels; dissipating diodes (that can also be used for thermal testing); sealing parts with gas inlet for different channel patterns.

2 WP2 - Simulation and modelling

In this work package mainly the thermal behavior of the microscale heatsink structure was investigated by multi-domain simulation and modelling. Some CFD simulations of different channel patterns were carried out and certain ones were selected and recommended for fabrication. The main aim was to generate a compact model of the integrated microscale heatsink structure which can be used in the future in thermal / electro-thermal simulation tools. Another important issue was to acquire a behavior model which is useful for system-level analysis, virtual prototyping etc. WP2 also interacted with WP3 as the outcome of the compact modelling and the electro-thermal simulations in the final phase was compared with the results of the characterization.

During the modelling and compact model generation tasks, the main aim was to create a ladder-type analytical thermal model for microscale channel based heatsink structures to determine the local heat transfer(s) and the temperature distribution along the channel(s) depending on the channel geometries, the thermal properties of the fluid and the wall temperature(s). However, the main difference between other solutions and our model is the fact that it deals with the hydrodynamic entry phenomenon and only includes analytical derivations.

During the model creation phase several considerations had to be made, since the resulting model have to be “simple” or compact enough to be used even in conventional electrical circuit simulator programs. However, the heat transfer and the temperature distribution along the channel cannot be described with one stage of a preferably RC model. In addition, several non-linearities and multiphysical coupling effects are to be considered as well.

An essential step to gain a model was the division of the channel into several segments and for each segment a T-equivalent circuit is created. The ladder-type thermal model obtained by applying the T-equivalent subcircuit as a building block can be used as a compact model of microscale channel structures. [4]

Several analytical or semi-empirical equations can be found in [5] to determine the average Nusselt number, which depends on the cross sectional geometry and the length of the channel These equations also deal with the hydrodynamic entry phenomenon, which describes the Nusselt number near the inlet, thus the heat transfer coefficient will be higher than the average Nusselt number of the whole channel.

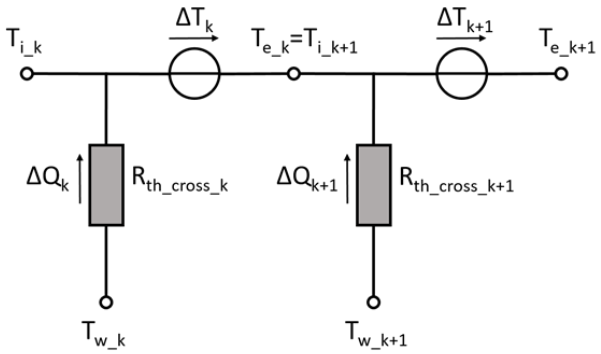


Figure 3 The proposed T-equivalent analytical thermal model of one channel (two neighbouring segments are depicted)

Based on our calculations an equivalent circuit model can be created (Figure 3) which can be applied in conventional electrical simulator tools. It is based on the analogy between the thermal and electrical systems. The temperatures and the heat flow rates can be corresponded to the voltage and electrical current values respectively. This model consists of a *heat flow controlled temperature source* which represent the convective heat transfer between wall and fluid.

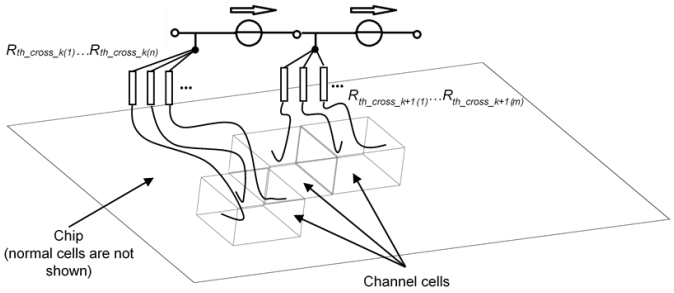


Figure 4 Channel model implemented as boundary condition for the SUNRED model

This model was implemented in a conventional thermal field solver (CTFS) simulation tool to augment the capability of simulating the thermal impact of integrated heat sink structures even with radial channel pattern. The implementation steps and the results are compared to the analytically calculated, CFD modelled and to the measured values. This augmented CTFS engine gives the opportunity to investigate the operation of System-on-Package (SoP) devices by electro/logi-thermal simulation.

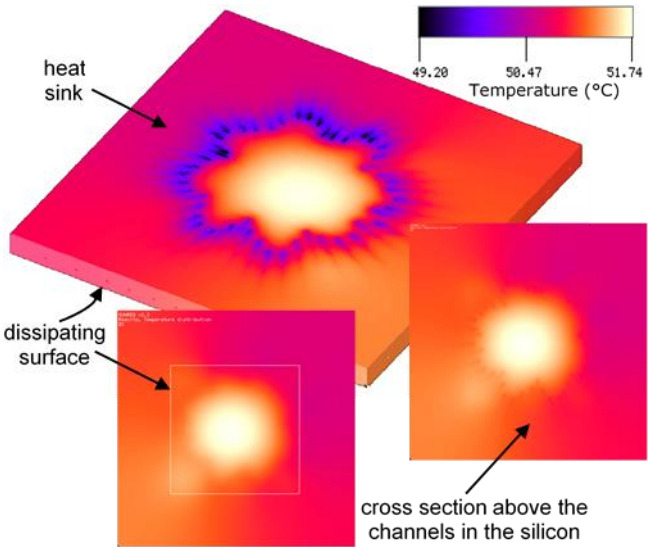


Figure 5 Temperature distributions from SUNRED simulation of the realized structure, volumetric flow rate = 120 l/h

Our novel analytical fluid dynamics compact models can be used in logi- or electro-thermal simulation tools to determine the *flow, pattern, fluid properties, etc. dependent* local heat flux and the temperature distribution on the surface of the chip even in

case of stacked-die structures. The new compact model can take the variable Nusselt values along each channel into account which is very important in the proper, thermal aware placement of the dissipating components. A thermal simulator tool was extended with the presented compact models to make it eligible to accurately simulate the hydrodynamics phenomenon in a short time. This extended thermal simulator engine was connected to the logic simulator engine creating Logi-thermal simulation capabilities. Nonetheless, this environment can provide insights to the temperature-dependent behavior of the circuit it can give additional details about dynamic thermal characteristics of the digital circuit.

3 WP3 - Characterization

The WP3 focused on the characterization and verification of microchannel cooling structures. In the first phase the development of a new measurement setup and support structure for thermal transient testing was done. The main goals were to measure the partial thermal resistance of the microchannel cooling structures with different build-ups and patterns and compare these results to the results of the simulation and modelling work of WP2. In this way, a new multi-domain characterization method of different microfluidic channel based heat exchanger structure was created.

The first set of samples were manufactured with the microscale channels only, which means that no active device was realized on the top side of the wafer (Figure 6). As a consequence, the thermal characterization of the foreseen cooling solution at this stage required the application of an external active device.

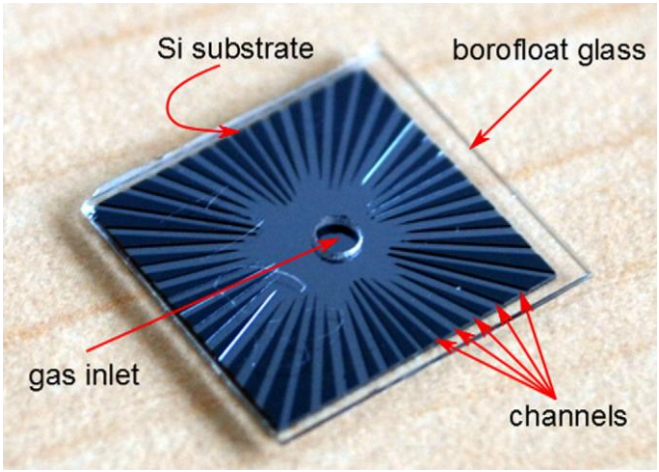


Figure 6 The first prototype of the microscale heat exchanger with radial channel pattern

The thermal resistance was measured by attaching a high-power transistor acting as a heater and simultaneously a temperature sensor to one side of the structure, and a cold-plate to the opposite side providing the thermal ground (Figure 7).

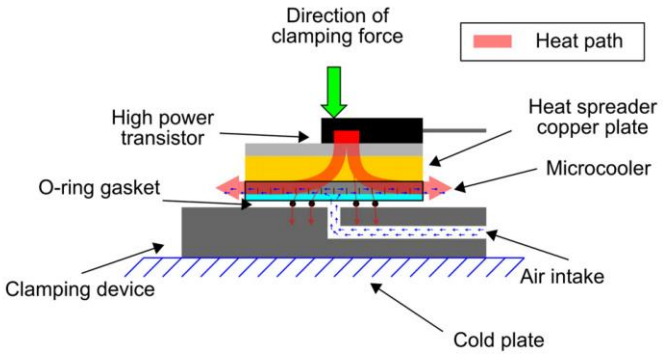


Figure 7 Cross-sectional view of the improved sample holder of the measurement setup

The method of obtaining the partial thermal resistance of the microchannel heat sink is identified with the help of the structure functions. In order to obtain the structure function, thermal transient measurement has been carried out. The recorded thermal transient contains all available information about the 1D heat-conduction path. In our case this path starts at the junction of the power transistor and ends at the thermal ground (cold plate, micro-channel cooler).

The concept of extracting information from the thermal transient was already introduced several years ago and was described in a number of publications and standards [6]-[8]. The cumulative structure function is a direct map of the cumulative thermal

capacitance vs. cumulative thermal resistance from the junction of the transistor to the cold plate [9].

The flow rate of the cooling fluid was controlled by a digital mass flow control unit. As a result of the measurements we managed to determine the thermal resistances at different flow rates. These results are in good agreement with the analytical calculations and the CFD simulations.

In the 2nd part of the research project several additional, previously unexplored measurement error sources were identified and resolved. The main error source was caused by the outflowing of the heated-up fluid. Since the speed of the outlet gas was significant, it induced pressure difference in the surroundings which moved the air in the vicinity of the measurement structure. As a consequence, the moving air near the structure created a parallel heat flow that tampered the measurement results, which generated a flow rate dependent convective heat exchange (Figure 8).

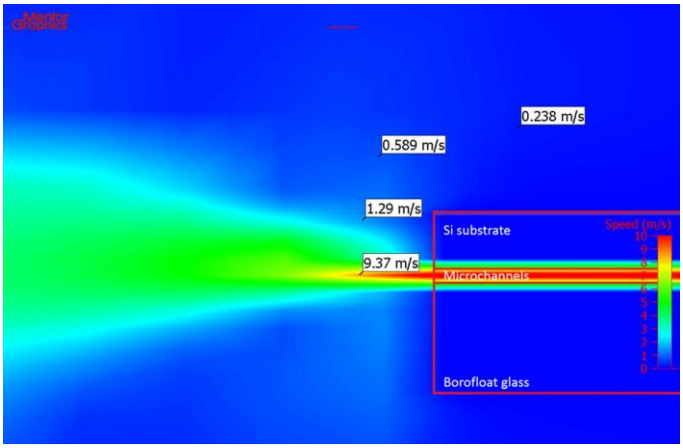


Figure 8 Air velocity map around the outlet of the sample holder

Based on these new results the measurement setup was refined (Figure 9) and new measurements were carried out. With the new measurement system, (Figure 10) numerous measurement errors have been eliminated. The measured results were compared to the CFD simulation results and gave a very good correspondence, better then in case of the former results.

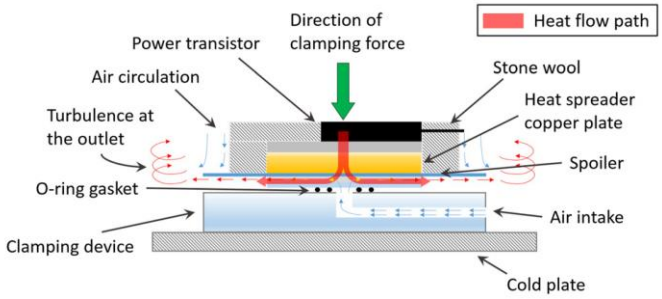


Figure 9 Cross-sectional view of the enhanced sample holder of the measurement setup

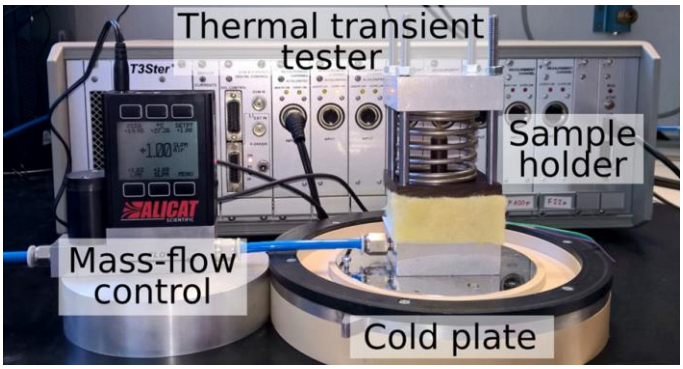


Figure 10 The enhanced measurement setup

With this new measurement setup, the hydrodynamic and the thermal characterization for the new samples were carried out by using liquid and gas coolant, as well.

Thanks to the new measurement setup, the determined partial thermal resistance values could have been compared to the results

of the simulations and analytical calculations. The highest deviation was 8% at 30 litres per hour but with increasing flow-rates the measurement errors become lower, that is quite an outstanding in case of microscale thermo-hydrodynamic characterization.

4 WP4 - Characterization of concentrated photovoltaic cells (CPV) and other applications

In the beginning of the research period the applicability of cooling structures with integrated microscale channels only in SoP structures were investigated. It was evident that in the first years we concentrated much effort to advise integration possibilities since the successful integration would be a real breakthrough. It was found out that companies like IBM are also having difficulties with this step.

The main problem with System-on-Package (SoP) structures is that different dies are stacked on each other forming a real 3D structure. Between the dies, high resistivity layers are formed to ensure electrical insulation. These layers also have high thermal resistivity and therefore the temperature elevation is higher beside the same dissipation.

One way to decrease the thermal resistance is to bring the cooling structures closer to the junction that is why it has to be realized inside the package. In our approach, the microscale channel structure is realized inside the die itself which results lower thermal resistance between the active area and the case/ambient.

It can be imagined that the elaborated characterization method, simulation engine and the manufacturing have numerous applicability. As it was described, we envision its usage in System-on-Package devices, stacked-die structures to decrease the thermal resistance of the primary heat flow path. Despite the fact that the first demonstrator SoP device which utilizes microscale heatsink structures is still in development, we have looked towards other areas to demonstrate the expedience of our method.

During the last phase of the project the applicability and the realization possibilities of the integration of microscale channel based heat sink structures to the Concentrated Photovoltaic Cells for integrated thermostating purpose were investigated (Figure 11). [10]

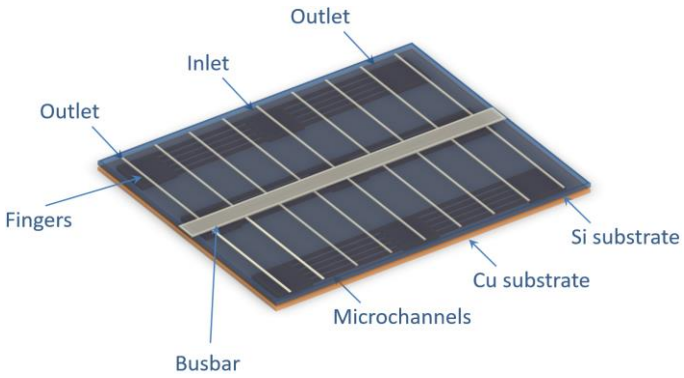


Figure 11 Visualization of the CPV cell

Based on the results of WP2, the maximum heat flux could have been estimated in case of different channel patterns and different types of coolant before the fabrication. The geometries (height, length of the channel, etc.) were optimized regarding to thermal and fabrication aspects. By applying water as a liquid coolant beside applying 1 bar pumping power the maximum achievable heat flux is calculated and simulated to be up to 300W from a $5\,\text{cm} \times 5\,\text{cm}$ area. The process steps were developed and the demonstrational sample was fabricated (Figure 12).

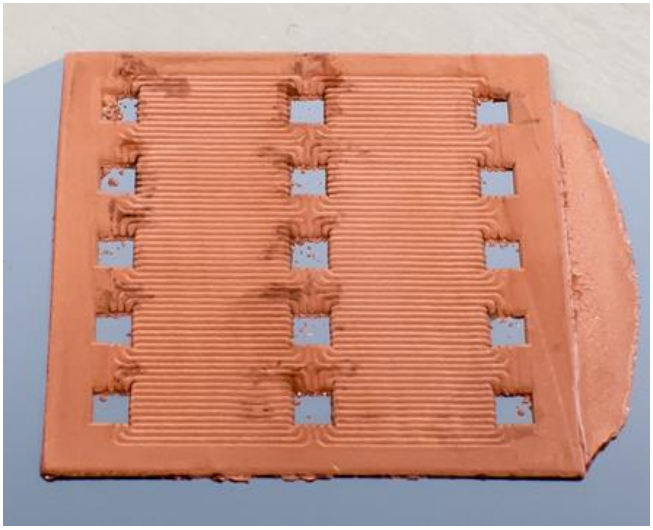


Figure 12 First CPV prototype

In our concept, the microscale channels can be integrated into the back surface metallization. The microscale channels can be formed by electroplating copper around a photoresist channel pattern. This approach has the advantage that it has no restrictions regarding the solar cell material and technology. Our research team developed a detailed description on the process technology, performed mechanical simulations for the feasibility of our approach, optimized the channel geometry for a 20×20 mm concentrator solar cell and estimated the cooling performance of the microscale channel structure at different operating conditions. We found that the proposed cooling solution can be applicable. The characterization and the measurement of the samples are in progress.

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